REMARKS

Claims 1-4 are all the claims pending in the application. Reconsideration and allowance of all the claims are respectfully requested in view of the following remarks.

Personal Interview

Applicants thank the Examiner for the courtesy extended to their representative during the personal interview conducted on October 10, 2003. During the Interview, Applicants' representative discussed the advantages of recognizing a chip when it is in a position as set forth in claims 1 and 4, as well as argued that Shibata, Abe, and JP '286 fail to teach or suggest such a feature in combination with the other elements as claimed. The Examiner indicated that such a function should be more closely tied to structure within the claim, and Applicants' representative indicated that such an amendment would be considered. No specific amendments to the claims were discussed. Applicants' representative then discussed the advantages of locating a chip tray in the manner as set forth in claim 3. The Examiner indicated that such a positioning of the chip tray is distinguishable from the teachings of the prior art.

By this amendment, Applicants have implemented the Examiner's suggestion as discussed in the personal interview and, therefore, Applicants respectfully request that the Examiner enter and consider this amendment made after Final Office Action.

Claim Rejections – 35 U.S.C. § 103

The Examiner rejected claims 1-3 [sic][1] under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,193,132 to Shibata et al, (hereinafter Shibata), in view of U.S. Patent 5,803,341 to Abe (hereinafter Abe), or Japanese 6-69286 (hereinafter JP '286). Applicants respectfully traverse this rejection for the following reasons.

[1] According the Office Action, page 2, section 3, only claims 1-3 where rejected, however in this same section the Examiner discusses the location of the chip within ± 5 mm of plane of the substrate, which is found in Claim 4. This is likely a clerical error and the Examiner probably meant to include claim 4 in the statement of the rejection.

First, the references fail to teach or suggest all the elements as set forth in Applicants' claims.

The arguments made in the May 27 Amendment are still pertinent and, therefore, are incorporated herein by reference.

Further, claim 1 sets forth a bonding apparatus comprising a chip recognition camera disposed lower than a level of a substrate mounted surface of a substrate stage to thereby recognize the chip held by the bonding tool from a position below the chip, wherein the chip recognition camera is focussed so as to recognize a lower surface of the chip, when the lower surface of the chip is located substantially on a level with a chip bonding surface of the substrate.

In Shibata, the chip picked up by the bonding tool 12 is recognized by the first recognition camera 14, and thereafter the provisional bonding is performed based on the recognition result. Then, the reference mark of the substrate and the chip are detected by the second recognition camera 16 to seek the positional relationship between the substrate and the chip. This is a teaching operation. See column 6, line 10 to 62. Thereafter, the actual bonding is performed, and finally a shift amount of bonding is detected to thereby judge OK or NB of the bonding operation. See column 6, line 63 to column 7, line 40.

In contrast to the present invention as set forth in claim 1, in Shibata's apparatus the lower surface of the chip is not located substantially on a level with a chip bonding surface of the substrate. Further, although the chip 13 is recognized by the first recognition camera 14 in Shibata, it must judge OK or NG of the bonding due to bonding shift amount. Such judgement of the bonding inherently indicates that the bonding shift owing to the shift of the bonding axis (ball screw, guide, etc.) is necessarily caused as described in the background section of the present application. And Shibata never teaches or discloses specific solutions to solve that problem. In other words, because Shibata gets errors in positioning, it does not inherently recognize the chip when the chip is in substantially the same plane as the bonding surface of the substrate. And there is no motivation to recognize the chip when the lower surface of the chip is located substantially on a level with a chip bonding surface of the substrate as set forth in the claimed invention to eliminate the shift amount. To the extent that the Examiner is relying on measurements from Shibata's figures, such is impermissible because there is no indication that

the drawings are to scale. And proportions of features in a drawing are not evidence of actual proportions when drawings are not to scale. When a reference does not disclose that the drawings are to scale and is silent as to dimensions, arguments based on measurement of the drawing features are of little value. MPEP § 2125.

In Abe, the TCP 17 held by the nozzle 16 (bonding tool) is moved to the focus range A in Figs. 2 and 3 of the camera 4, and the positioning object 18 of the TCP 17 is recognized. Then, the nozzle 16 is moved outward (column 5, line 57 to column 6, line 38). Next, the positioning object 2 of the LCD 1 is moved within the focus range A of the camera 4 (column 6, line 40-55) to thereby correct the mounting position based on the recognition results.

In contrast to the present invention, the following points are different:

i) moving the chip within the focus range is not the same as locating the chip substantially on a level with the substrate at the recognition by the camera since a certain physical range exists in the focus range, the lower surface of the chip is not located substantially on a level with a chip bonding surface of the substrate; and

ii) only one camera 4 is provided and bonding is not performed by two cameras (chip recognition camera and substrate recognition camera).

Second, the Examiner has failed to do his job by not responding to Applicants' arguments as set forth in the Amendment filed on May 27, 2003.

Specifically, the Examiner has not complied with the procedure for Examination of Applications under MPEP § 706.02 (j), which states, it is important for an Examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply. That is, the Examiner is required to explain why one of ordinary skill in the art at the time of the invention would have been motivated to make the proposed modification.[2] In this regard, the Examiner failed to address the arguments made in the

[2] MPEP § 706.02, *see* page 700-45 item (D).

May 27 Amendment.[3] For example, the Examiner did not respond to Applicants' argument that neither Shibata nor Abe teaches or suggests a chip source as claimed by the Applicants.

Third, the references fail to establish prima facie obviousness of claim 4 for the following reasons.

Claim 4 sets forth that a chip recognition camera is focussed so as to recognize a lower surface of the chip when the lower surface of the chip is located within ± 5 mm of a plane in which is located a chip bonding surface of a substrate.

The Examiner asserts that Shibata teaches a substrate recognition camera (16) disposed above the substrate stage, as well as that the chip and the substrate are subject to positioning on the basis of recognition results from the chip recognition camera and the substrate recognition camera. According to the Examiner, the chip recognition camera is *capable* of locating the chip within ± 5mm of a plane of the substrate. The Examiner mistakenly believes that if the chip recognition camera in the prior art is capable of doing what is claimed then there is sufficient basis for an obviousness rejection. According to MPEP §2143.01, however, although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so."[4] Regardless of whether the recognition camera in Shibata is capable of locating a chip within ± 5mm of a plane of a substrate, the Examiner must provide "a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teaching of the references."[5] Simply because the prior reference may be capable is not enough. The burden is on the Examiner to point to areas in Shibata and Abe that would lead one skilled in the art to recognize a chip when it is within ± 5mm of the plane of the substrate. Because the location of Shibata's camera, chip, and substrate, are not immediately apparent, it is the duty of Examiner to explain why this would be obvious under 35 U.S.C. § 103(a), *see* MPEP § 2142. This the Examiner has not done.

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[3] *See* Amendment of May 27, 2003 page 5.

[4] MPEP § 2143.01 *citing* In re Mills, 916 F.2d 680, 682, 16 U.S.P.Q.2d 1430,1432 (Fed. Cir. 1990).

[5] MPEP § 2142 *citing* Ex parte Clapp, 227 U.S.P.Q 972, 973 (Bd. Pat. App. & Inter. 1985).

For at least any of the above reasons, Shibata, Abe and JP '286 fail to render obvious Applicants' claims 1-4.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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